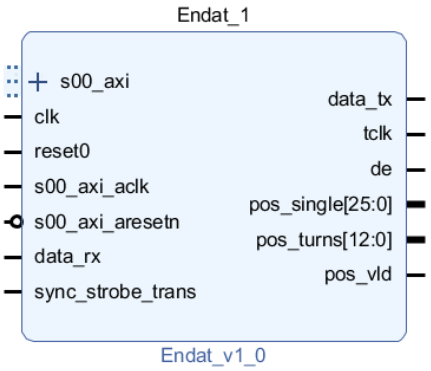
Endat 2.1/2.2 Master Module (APB 32bits Interface)

By Dr. Qielu Pan March, 2022

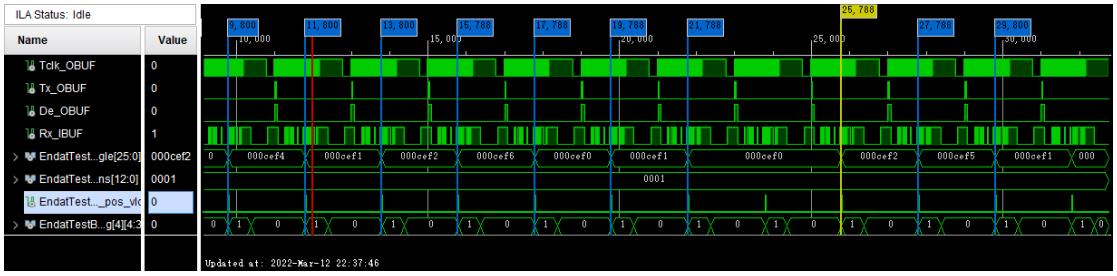
Dr. Pan developed this Endat master module independently based on Xilinx FPGA. It supports Endat 2.1/2.2 protocol. We can provide a time-limited version and related initial program for your test.



The main parameters of the module are as follows:

No.	Items	Value
1	Input clock	100MHz
2	CPU Interface	ARM APB 32bits
3	Max. Singleturn Resolution	26bits
4	Max. Multiturn Resolution	13bits
5	Transmission Rate	200KHz ~ 16.67MHz
6	Strobe type	Software/Timer/Hardware

Test results: (8.33MHz, Timer strobe)



Test results: (16.67MHz, Software strobe)